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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/550,876	09/27/2005	David A. Fish	GB 030031	1759

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EXAMINER	
TRAN, MY CHAU T	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
09/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,876	FISH ET AL.	
	Examiner	Art Unit	
	MY-CHAU T. TRAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,10,11,13 and 14* is/are rejected.

7)☒ Claim(s) *4-9,12 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application and Claims Status

1. Applicant's amendment and response filed 07/02/2008 are acknowledged and entered.

2. Claims 1-15 were pending. Applicants have amended claims 1-15. No claims were added and/or cancelled. Therefore, claims 1-15 are currently pending and are under consideration in this Office Action.

Status of Claim(s) Objection(s) and /or Rejection(s)

3. The objection of claims 1-15 has been withdrawn in light of applicant's amendments of claims 1-15 thereto.

4. Please note that the following action has been made non-final in view of the fact that the indicated allowability of claims 10 and 11 are withdrawn upon further reconsideration, and new grounds of rejection is made in view of Fish et al. (US Patent Application Publication US 2006/0208979 A1).

New Rejection(s)

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for

patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Dawson et al. (US Patent 6,229,506 B1).

For ***claims 1-3 and 13***, Dawson et al. disclose a variety of active matrix light emitting diode (LED) pixel structure for an active matrix display (see e.g. Abstract; col. 2, lines 13-25; figs. 1-4 and 6). The active matrix display is art recognized to comprise an array of display pixels (see e.g. col. 1, lines 19-27; fig. 1). In one embodiment as illustrated figure 3, the LED pixel structure comprises four transistors (ref. #360, 365, 370, and 375), two capacitors (ref. #350 and 355), and a LED (ref. #OLED) (refers to instant claimed light emitting display element and instant claim 13) (see e.g. col. 4, lines 41-55). The transistor (ref. #375) (refers to instant claimed first driving transistor) and the LED (ref. #OLED) are connected in series between the power line (ref. #390) and data line (ref. #310) that provide both reference and data voltages (refers to instant claimed power supply lines) (see e.g. col. 4, lines 41-67; fig. 3). The capacitor (ref. #350) (refers to instant claimed second capacitor) is connected to the gate of transistor (ref. 365) (refers to instant claimed second transistor) (see e.g. fig. 3). The capacitor (ref. #355) is connected to both the transistor of reference characters 375 and 365 (refers to instant claim 2). The transistor (ref. #360) (refers to instant claimed address transistor) is connected to the data line (ref. #310) (refers to instant claimed data input line) and the select line (ref. #320) (refers to instant claimed input to the pixel) (see e.g. fig. 3). In addition, Dawson et al. also disclose the driving method of this active matrix display wherein the transistor (ref. #365) is isolated during the auto zero phase and it is not isolated during the load data phase and illuminating phase, (i.e.

the programming phases) (see e.g. col. 5, lines 1-31). This implies that transistor (ref. #365) can perform the function as claimed in claim 1 regarding the newly added functional limitation of "*operable only during pixel programming*".

For ***claim 14***, Dawson et al. disclose a variety of active matrix light emitting diode (LED) pixel structure for an active matrix display (see e.g. Abstract; col. 2, lines 13-25; figs. 1-4 and 6). As illustrated by figure 2 of one embodiment, the LED pixel structure comprises four transistors (ref. #240, 250, 260, and 270), and transistor (ref. #260) (refers to instant claimed first drive transistor) is connected to a capacitor (ref. #280) (refers to instant claimed first storage capacitor) and a LED (ref. #290/OLED) (refers to instant claimed light emitting display element) (see e.g. col. 3, lines 11-22). Dawson et al. also disclose the driving method of this active matrix display wherein the method comprises steps of using an input voltage to drive a second drive transistor (ref. #240); passing the source drain current through the first drive transistor (ref. #260); storing the gate-source voltage of the first drive transistor resulting from passing the source drain current through the first drive transistor on a first storage capacitor (ref. #280); driving the display element (ref. #290) using the first drive transistor based on the stored gate-source voltage; and switching off the second drive transistor (see e.g. col. 3, line 30 thru col. 4, line 5).

Therefore, the device and method of Dawson et al. do anticipate the instant claimed invention.

Response to Arguments

7. Applicant's arguments directed to the above 102(b) rejection were considered but they are not persuasive for the following reasons. Please note that the above rejection has been

modified from it original version to more clearly address applicant's newly amended and/or added claims and/or arguments.

[1] Applicant contends that Dawson et al. do not teach the newly added limitation "*that the second drive transistor is operable only during pixel programming. Support for this feature is found, inter alia, in the published specification at paragraph [0055]*" of claim 1.

[2] Applicant alleges that in regard to claim 14 "*the feature "switching off the second drive transistor" when taken in conjunction with the claim's preamble recitation of "a method of addressing an active matrix display device" is comparable to the above described analysis of amended claim 1. That is, the second drive transistor is only operable during the addressing phase (or "programming" phase as defined in paragraph [0053])*".

Thus, the teachings of Dawson et al. do not anticipate the device and method of the instant claims.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. It is the examiner's position that Dawson et al. do disclose the device's limitations of instant claimed claim 1. First, the device of Dawson et al. meets all the structural limitations of the claimed device of instant claim 1, i.e. a light emitting display element and first drive transistor are in series between the power supply lines, a first storage capacitor connected to first drive transistor, and a second drive transistor connected to the first drive transistor and second capacitor, as discussed above in paragraph 6 above. Second, the newly added functional limitation, i.e. "*is operable only during pixel programming*", does not impart any structural distinction between the instant claimed second drive transistor and the

transistor of reference #365 of figure 3 of Dawson et al. See MPEP § 2114, which states as follows:

> *APPARATUS CLAIMS MUST BE STRUCTURALLY DISTINGUISHABLE FROM THE PRIOR ART*
> **>While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function.** *>In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997)* (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also *In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971); < In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).* "[A]pparatus claims cover what a device is, not what a device does." *Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990)* (emphasis in original).
>
> *MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART*
> **A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim.** *Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).*

Moreover, Dawson et al. also disclose the driving method of this active matrix display wherein the transistor (ref. #365) is isolated during the auto zero phase and it is not isolated during the load data phase and illuminating phase, (i.e. the programming phases) (see e.g. col. 5, lines 1-31). This implies that transistor (ref. #365) can perform the function as claimed in claim 1 regarding the newly added functional limitation of "*operable only during pixel programming*". Consequently, Dawson et al. do disclose the instant claimed limitations of claim 1.

[2] The examiner respectfully disagrees. It is the examiner's position that Dawson et al. do disclose the method of instant claim 14. First, Dawson et al. do disclose the method of instant claim 14 as discussed above in paragraph 6 wherein the method comprises the step of "*switching off the second drive transistor*". Second, applicant asserts that a) the instant claimed method of claim 14, i.e. a method of addressing an active matrix display device, is interpreted as a method for 'programming'/driving an active matrix display device; and b) the instant claimed step of

"*switching off the second drive transistor*" of claim 14 and the newly added functional limitation of "*operable only during pixel programming*" of claim 1 would distinguished the instant claimed device from the device of Dawson et al. However, a) the examiner does not dispute that the instant claimed method of claim 14, i.e. a method of addressing an active matrix display device, can be interpreted as a method for 'programming'/driving an active matrix display device for Dawson et al. also disclose a method for driving an active matrix display device as discussed above in paragraph 6; and b) it is the examiner's position that the instant claimed step of "*switching off the second drive transistor*" of claim 14 and the newly added functional limitation of "*operable only during pixel programming*" of claim 1 does not impart any structural distinction between the instant claimed second drive transistor and the transistor of reference #365 of figure 3 and/or reference #240 of figure 2 of Dawson et al.

Therefore, the teachings of Dawson et al. do anticipate the device and method of the instant claims, and the rejection is maintained.

8. Claims 1-4, 10, 11, 13, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Fish et al. (US Patent Application Publication US 2006/0208979 A1; *Effective filing date of 02/27/2004*).

The applied reference has common inventors, i.e. David A. Fish and Jason R. Hector, with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

For ***claims 1-3 and 13***, Fish et al. disclose a variety of active matrix light emitting diode (LED) pixel structure for an active matrix display (see e.g. Abstract; sections: [0017]-[0024], and [0027]-[0029]; figs. 4, 6, 8, 11, 13, 14, 16, 18, 20, 22, and 24). In one embodiment as illustrated by figure 18, the LED pixel structure comprises six transistors (ref. #16, 22, 34, 36, 62, and 121), three capacitors (ref. #30, 40, and 120), and display element (ref. #2) that is an LED (refers to instant claimed light emitting display element and instant claim 13) (see e.g. sections: [0104]-[0112]). The transistor (ref. #16) is an addressing transistor (refers to instant claim 18) that is connected to the row conductor (ref. #4) (refers to instant claimed input) and the column conductor (ref. #6) (refers to instant claimed data input line) (see sections: [0007], [0070], [0114]; figs. 2, 3, 4, and 18). The transistor (ref. #22) (refers to instant claimed first driving transistor) is connected to the display element (ref. #2) and the power supply line (ref. #26) in series (see e.g. fig. 18). The capacitor (ref. #30) (refers to instant claimed first storage capacitor and instant claim 2) is between the transistor (ref. #22) (refers to instant claimed first driving transistor) and transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. fig. 18). The capacitor (ref. #40) (refers to instant claimed second storage capacitor) is connected to the transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. fig. 18). The threshold voltage capacitor (ref. #120) is between the capacitor (ref. #40) (refers to instant claimed second storage capacitor) and the transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. section: [0112]; fig. 18).

For ***claims 10 and 11***, Fish et al. disclose Fish et al. disclose a variety of active matrix light emitting diode (LED) pixel structure for an active matrix display (see e.g. Abstract; sections: [0017]-[0024], and [0027]-[0029]; figs. 4, 6, 8, 11, 13, 14, 16, 18, 20, 22, and 24). In

one embodiment as illustrated by figure 18, the LED pixel structure comprises six transistors (ref. #16, 22, 34, 36, 62, and 121), three capacitors (ref. #30, 40, and 120), and display element (ref. #2) that is an LED (refers to instant claimed light emitting display element and instant claim 13) (see e.g. sections: [0104]-[0112]). The transistor (ref. #16) is an addressing transistor (refers to instant claim 18) that is connected to the row conductor (ref. #4) (refers to instant claimed input) and the column conductor (ref. #6) (refers to instant claimed data input line) (see sections: [0007], [0070], [0114]; figs. 2, 3, 4, and 18). The transistor (ref. #22) (refers to instant claimed first driving transistor) is connected to the display element (ref. #2) and the power supply line (ref. #26) in series (see e.g. fig. 18). The capacitor (ref. #30) (refers to instant claimed first storage capacitor and instant claim 2) is between the transistor (ref. #22) (refers to instant claimed first driving transistor) and transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. fig. 18). The capacitor (ref. #40) (refers to instant claimed second storage capacitor) is connected to the transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. fig. 18). The threshold voltage capacitor (ref. #120) (refers to instant claimed voltage compensation circuitry/third capacitor and instant claim 11) is between the capacitor (ref. #40) (refers to instant claimed second storage capacitor) and the transistor (ref. #36) (refers to instant claimed second driving transistor) (see e.g. section: [0112]; fig. 18).

For ***claim 14***, Fish et al. disclose a driving method for the active matrix display of figure 18 (see e.g. sections: [0113]-[0116]). The method comprises the steps of using an input voltage to drive a second drive transistor (ref. #36); passing the source drain current through the first drive transistor (ref. #22); storing the gate-source voltage of the first drive transistor resulting from passing the source drain current through the first drive transistor on a first storage capacitor

(ref. #30); driving the display element (ref. #2) using the first drive transistor based on the stored gate-source voltage; and switching off the second drive transistor (see e.g. sections: [0113]-[0116]).

Therefore, the devices of Fish et al. do anticipate the instant claimed invention.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claim 1 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4, and 6 of copending Application No. 10/548,343 (US Patent Application Publication US 2006/0208979 A1; hereinafter refers to as Fish et al.). Although the conflicting claims are not identical, they are not patentably distinct from each other because both the apparatus of the instant claim 1 and the apparatus of claims 1, 4 and 6 of Fish et al. have similar structural features.

Specifically, claim 1 of Fish et al. claimed an active matrix display device comprising a current-driven light emitting display element (refers to instant claimed light emitting display element), a drive transistor (refers to instant claimed first driving transistor) for driving a current through the display element, a storage capacitor (refers to instant claimed first storage capacitor) for storing a voltage to be used for addressing the drive transistor; and a discharge transistor (refers to instant claimed second driving transistor) for discharging the storage capacitor thereby to switch off the drive transistor. Claim 4 claimed a discharge capacitor (refers to instant claimed second storage capacitor) is provided between the gate of the discharge transistor and a constant voltage line. Claim 6 claimed the drive transistor is connected between a power supply line and the display element. That is the apparatus of the instant application is generic to the apparatus of Fish et al. or in other word claim 1 are anticipated by claims 1, 4, and 6 of copending Application No. 10/548,343 (US Patent Application Publication US 2006/0208979 A1). Consequently, the examined claims would be obvious over the claims of copending Application No. 10/548,343 (US Patent Application Publication US 2006/0208979 A1).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

11. Claims 4-9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is (571)272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/MY-CHAU T. TRAN/
Primary Examiner, Art Unit 2629

September 19, 2008